**AMENDMENTS TO THE CLAIMS**

**1.** (Currently Amended) A semiconductor device having a self-aligned contact hole, the device comprising:

a substrate;

a first conductor structure and a second conductor structure formed on the substrate;

an insulator structure formed on the first and second conductor structure and on the substrate except over the substrate in a region between the first and second conductor structures; and

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sidewall spacers, each sidewall spacer being formed to abut against both a side of the first or second conductor structures and a side of the insulator structure such that a vertical portion of each sidewall spacer abuts the conductor structures, the sidewall spacers manifesting the self-aligned contact hole in the region between the first and second conductor structures, wherein the self-aligned contact hole does not overlap any part of the first and second conductor structures.

**2.** (Original) The semiconductor device of claim 1, wherein the first and second conductor structures are first and second gate structures, respectively.

**3**. (Original) The semiconductor device of claim 1, wherein the first and second conductor structures comprise:

a gate oxide layer formed on the substrate;

a conductive layer formed on the gate oxide layer; and

a gate cap insulating layer formed on the conductive layer.

**4**. (Original) The semiconductor device of claim 1, further comprising:

a contact plug formed in the self-aligned contact hole.

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**5**. (Currently Amended) An unsymmetrical semiconductor device using a self-aligned contact hole, the device comprising:

a substrate having impurity regions formed therein;

a first conductor structure and a second conductor structure formed on the substrate;

first sidewall spacers, each first sidewall spacer being formed to abut against both a side of the first or second conductor structures and a side of an insulator structure such that a vertical portion of each sidewall spacer abuts the conductor structures, the first sidewall spacers manifesting the self-aligned contact hole in the region between the first and second conductor structures, wherein the self-aligned contact hole does not overlap any part of the first and second conductor structures; and

second sidewall spacers formed on sides of the first and second conductor structures opposite of the self-aligned contact hole.

**6**. (Original) The unsymmetrical semiconductor device of claim 5, wherein the ion concentration of a first impurity region is different than the ion concentration of a second impurity region.

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**7**. (Currently Amended) The unsymmetrical semiconductor device of claim ~~5~~ 6, further comprising:

a contact plug formed in the self-aligned contact hole, the contact plug being in contact with the first sidewall spacers and the first impurity region.

**8**. (Original) The unsymmetrical semiconductor device of claim 7, wherein the contact plug is also in contact with a bit line.

**9**. (Original) The unsymmetrical semiconductor device of claim 7, wherein the contact plug is not disposed directly above the first and second conductor structures.